AMENDMENTS TO THE SPECIFICATION

In the Specification

Please substitute the following amended paragraph(s) and/or section(s) (deleted matter is shown by strikethrough and added matter is shown by underlining):

Page 1, line 7-line 14:

RELATED APPLICATIONS

The applicants hereby claim benefit of the contents and filing date accorded to U.S. Provisional Patent Application filed August 1, 2000 as Serial No. 60/222,256 and entitled, "High Receiver Sensitivity Transceiver." The present invention is related to co-pending application assigned to the assignee of the present invention and entitled "Spread Spectrum Meter Reading System Utilizing Low-Speed/High Power Frequency Hopping", filed July 23, 2001, Serial No. 09/~~xxx,xxx~~ 911,840 ~~(Attorney Docket No. 1725.123-US-02)~~, the disclosure of which is hereby incorporated by reference.

Page 5, line 21 through Page 6, line 8:

SUMMARY OF THE INVENTION

A wireless spread spectrum communication system for transmitting data includes a plurality of end point transmitters and at least one receiver. The end point transmitters transmit data via a frequency hopped spread spectrum signal where the transmitting signal is sent without the benefit of frequency stabilization. The receiver is responsive to the frequency hopping spread spectrum signals and includes a correlator and a signal processor. The correlator samples

at least a first portion, e.g., 34 chips, of a preamble of the signal and correlates the portion of the preamble with a known preamble pattern to determine a probability of correlation. The signal processor applies a Fast Fourier Transform (FFT) algorithm to the signal in response to the probability of correlation to track a narrowband frequency of the signal based on at least a second portion, e.g., the last 6 chips, of the preamble and to decode data encoded within the signal subsequent to the preamble.

Page 17, line 17 through Page 18 line 3:

The components of the receiver board 42 of Figure 4 of a preferred embodiment of the present invention also include a RF amplifier ~~70that~~ 70 that preferably is comprised of two linear amplifiers (LNA) and a surface acoustic wave filter (SAW) to produce a 30 dB gain and a 1.2 dB NF. One of the LNAs has an NF of .9 db, a P1dB of -22dBm, and an IP3 of -10dBm. The other LNA has an NF of 1.6 dB, gain of 17 dB, P1dB of +12 dBm, and IP3 of 0 dBm. The mixer 74 preferably has a CG of +9 dB, a P1dB of -7dBm, and IP3 of -8dBm. The IF amplifier 76 preferably has a P1dB of 9.5dBm and NF of 5.5 dB. The IF filter 78 preferably has a bandwidth of 7 MHZ and an IL of 9 dB. The high speed A/D converter 64 is preferably a 12-bit converter operating at a rate of 16.384 MSPS, while the low speed A/D converter 66 is preferably a 12-bit converter that operates at a rate of 262.144 KSPS.

Page 20, line 8 through page 21, line 5:

As previously described, the RSSI voltage from the IF stage filter 78 is sampled with an A/D converter 66 and input to the DSP 52. Preferably, the sample is placed in a stack of samples internal to the DSP 52 with the oldest sample shifting out of the stack as the newest sample is

shifted in. preferably, [[he]] the stack is thirty four samples long, with each sample representing one of the bits of the preamble 42 to be correlated. It should be noted that the length of the stack is not critical to the performance of the present invention. Good correlations have been demonstrated using a subset of this number of samples. The number of samples (thirty-four) is really a subset of the entire ERT preamble 32 that is transmitted. After the new sample is taken and saved each sample in the stack is compared to a value representing the known and expected preamble. In a preferred implementation, if the known value of a bit of the preamble 32 is expected to be a binary one, it is assigned a value of one, whereas if the known value is expected to be a binary zero, the bit is assigned a value of negative one. The known value is compared by multiplying the unknown value from position one by the known value of position one. Then the unknown value of position two is multiplied by the unknown value of position two and so on until all thirty four unknown values have been multiplied by their corresponding known values. The results from all of the multiplications are then summed. This gives a correlation value to the current set of samples. Another sample is taken at the appropriate time and the whole process runs over again. The appropriate time is determined by the data rate of the ERT message. As previously described, in a preferred implementation the signal is oversampled 8 times so the list is 8 times longer as is the known bit list. The sampling rate is 8 times faster than the data rate as well. This allows the preferred embodiment to more accurately synchronize to the data.

Page 21, line 20 through page 22, line 15

Once a preamble is detected, there preferably are 8 chips remaining in the preamble 32 that have yet to be read. At this point, the high speed A/D converter 64 is activated. Although the A/D converter 66 could have been running all along, preferably the A/D converter 66 is

turned off to save power. The high speed A/D converter 66 samples the IF signal 70. The samples are then fed into the DSP 52, which runs a 64 point FFT to creates thirty two unique frequency bins 82, each 256kHz wide as previously described. Preferably, each frequency bin 82 is represented by a complex number that is converted into power by squaring the real and imaginary parts and adding them together. Starting this process takes a little time, so preferably the next two data samples of the incoming preamble are discarded. This leaves six bits of the incoming preamble that the expected state of is known. Since the DSP knows what ~~it looking~~ it is looking for, the DSP 52 examines the frequency bins 82 for the next six bit samples for the known pattern. When there is a bin 82 that contains a 101010 pattern (representing 12 known chips) in time with the expected preamble, that bin is [[label]] labeled as the best bin as described in connection with the description of Figure 5. This is essentially how the initial "frequency adjustment" is accomplished. It is not really adjusting a frequency, but rather it is determining the frequency where a transmission is occurring. Once the best bin is determined, the DSP uses the FFT algorithm to attempt decode the body 34 of the ERT message 30 on that channel. Since the ERT message30 contains a CRC error detection byte 36, it is possible determine a successful decode if the decode passes CRC check.